146/c 98

14

Reg. No.

18

Seventh Semester B.E. Degree Examination, February 2002

Electronics Engineering

VLSI Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Schematically represent the evolution of IC technology. **(5 Marks)**

   (b) Explain the working of an nMOS enhancement mode transistor with relevant sketches. **(5 Marks)**

   (c) Describe with neat sketches P well fabrication process for CMOS inverter. **(10 Marks)**

2. (a) Derive an expression for I_{ds} for an n MOS transistor in non-saturation and saturation regions. Draw $I_{ds}v/sV_{ds}$ curves indicating non saturation and saturation regions. **(12 Marks)**

   (b) Explain latching in case of CMOS devices with relevent diagram. **(4 Marks)**

   (c) What steps are taken to overcome latchup in case of CMOS devices? **(4 Marks)**

3. (a) Show that Z_{pu}/Z_{pd} for an n MOS inverter driven by another n MOS inverter is 4 : 1. **(8 Marks)**

   (b) Discuss four possible arrangements for pull ups in basic MOS transistors along with circuit diagrams and transfer characteristics. **(8 Marks)**

   (c) Draw an n MOS transistor model. **(4 Marks)**

4. (a) What are stick diagrams? **(4 Marks)**

   (b) Draw 2 input NOR gate circuit diagram using CMOS inverter along with monochromatic / colour stick diagram. **(8 Marks)**

   (c) Give λ based design rules with appropriate sketches for the following layers:

   i) Polysilicon layer.

   ii) Diffusion (n type) layer.

   iii) Metal 1 layer.

   iv) p type MOS transistor. **(8 Marks)**

5. (a) Define sheet resistance R_s and standard unit of capacitance and explain their significance. **(4 Marks)**

   (b) Deduce an expression for over all time delay t_d when a cascade of N even number of N MOS inverter is driving a large capacitance C_L. **(8 Marks)**

   (c) Calculate the total capacitance based on 5 micron technology for the structure

Contd.... 2

7. (a) Explain the general design procedure of 4-bit arithmetic processor. (6 Marks)

(b) Mention various VLSI design tools. Explain different levels at simulation of VLSI design. (6 Marks)

(c) Explain the following briefly :

i) Schematic design ii) Layout design

iii) Floor planning iv) Chip composition. (8 Marks)

8. Write short notes on

a) Threshold voltage of MOS transistor

b) Different forms of pullup

c) Silicides in MOS transistors

d) Devices available for driving large capacitive loads. (5×4=20 Marks)

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Reg. No.

Seventh Semester B.E. Degree Examination, January/February 2008

Electronics and Communication Engineering

VLSI Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) State Moore's I law. Classify and compare different I.C. Technologies. (8 Marks)

   (b) Explain the working of NMOS enhancement mode transistor with relevant sketches. (8 Marks)

   (c) Define the terms : i) Wafer ii) Mask iii) Polysilicon iv) Diffusion (4 Marks)

2. (a) Explain with neat sketches different steps involved in P-well fabrication process for CMOS inverter. (12 Marks)

   (b) Derive the expression of I_{ds} for an nMOS transistor in nonsaturation and saturation regions. (8 Marks)

3. (a) Prove that Z_{pu}/Z_{pd} ratio for an nMOS inverter driven by another nMOS inverter is 4:1. (6 Marks)

   (b) Explain the working of CMOS inverter with neat sketches. (8 Marks)

   (c) Describe the latch-up problem and its remedies in CMOS circuits. How does BiCMOS transistor is susceptible to latch-up problem? (6 Marks)

4. (a) What are stick diagrams? Explain the stick layout design of 1-bit shift-register and draw the same using stick diagram. (8 Marks)

   (b) Explain Lambda (λ) based VLSI design rules with suitable sketches. (12 Marks)

5. (a) Briefly describe the following terms : i) Sheet resistance ii) Standard unit of a capacitance iii) Delay unit τ (6 Marks)

   (b) Obtain the expression for overall delay τ_d for n number of cascaded pass transistors. (8 Marks)

   (c) Explain BiCMOS drivers. (6 Marks)

6. (a) What is the significance of scaling of MOS transistors? Explain different methods of scaling. (8 Marks)

   (b) Draw the circuit and stick diagram layout for two-input CMOS NAND gate. (6 Marks)

   (c) Explain the two basic ways: Switch logic and gate logic for building digital logic circuits in MOS technology. (6 Marks)

Contd.... 2

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CS/IS7H2

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Seventh Semester B.E. Degree Examination, January/February 2004

Computer Science/Information Science and Engineering

Distributed Computing

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Name four advantages and two disadvantages of distributed system over centralized one. (4 Marks)

   (b) With a neat diagram explain NFS layer structure. (10 Marks)

   (c) Explain different transparency features of a distributed system. (6 Marks)

2. (a) Differentiate between blocking primitives and non- blocking primitives. (8 Marks)

   (b) Explain Cristian's algorithm. Compare the same with Berkeley algorithm. (12 Marks)

3. (a) What is meant by mutual exclusion? Explain distributed and token ring algorithm. (10 Marks)

   (b) What is deadlock? Explain centralized deadlock detection procedure. (10 Marks)

4. (a) What are the design issues considered in implementing threads packages. (10 Marks)

   (b) Explain registry based algorithm for finding and using idle workstations with a neat diagram. (10 Marks)

5. (a) With a diagram explain amoeba system architecture. (10 Marks)

   (b) Explain any five process management primitives of Mach? (10 Marks)

6. (a) Explain the role of different types of networks used to support distributed systems. (10 Marks)

   (b) Briefly explain the different switching schemes. (10 Marks)

7. (a) What is RPC? With a neat diagram explain role of client and server stub procedures in RPC. (10 Marks)

   (b) What is interface definition language (IDL) ? How binding take place with the service? (10 Marks)

8. (a) What is meant by distributed query processing? Explain with examples. (10 Marks)

   (b) What are the file system requirements for distributed file system. (10 Marks)

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Seventh Semester B.E. Degree Examination, June 2007

Electronics and Communication Engineering

VLSI Design

Time: 3 hrs. [Max.Marks : 100

Note: 1. *Answer any FIVE full questions.*
2. *All questions carry EQUAL marks.*

1. (a) Discuss and compare the performance of available technologies for integrated circuits in terms of speed and power and their evolution. (8 Marks)

   (b) Describe with a neat diagram different steps involved in N-well process for CMOS fabrication. (12 Marks)

2. (a) Compare the performance of a pass transistor and a transmission gate. (5 Marks)

   (b) Derive the expression for I_{ds} for N-MOS transistor starting from basics. (10 Marks)

   (c) Discuss the latch-up problem in CMOS circuits. (5 Marks)

3. (a) Derive an expression for pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistor. (10 Marks)

   (b) Explain in detail the operation of CMOS inverter and derive an expression for V_{th} (10 Marks)

4. (a) What are stick diagrams? Draw the circuit and stick diagram for 2 I/P CMOS NOR circuit. (10 Marks)

   (b) Explain briefly λ based rules for wires, contacts and transistors. (10 Marks)

5. (a) Discuss different types of scaling in VLSI. (6 Marks)

   (b) Give the scaling factors for
   i) Gate area
   ii) Gate capacitance C_g
   iii) Gate delay
   iv) Channel Resistance
   v) Current density J.
   vi) Power - speed product P_T
   vii) Parasitic capacitance C_X. (14 Marks)

6. (a) Discuss Sheet Resistance (R_S) and area capacitance in a MOS transistor. (10 Marks)

   (b) Explain in brief the limitation of scaling. (10 Marks)

7. (a) Explain different types of CMOS logic. (10 Marks)

   (b) Briefly explain various design styles in VLSI design. (10 Marks)

8. Write short notes on:
   i) CAD tool for VLSI design (6 Marks)
   ii) 4-bit adder (6 Marks)
   iii) Design conditions for testability. (8 Marks)

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(c) Explain why only substrate doping 'N_B' has to be scaled up while all other parameters are scaled down. (4 Marks)

6. (a) What are switch logic and restoring logic circuits? Give one example for each. (4 Marks)

(b) Build and explain a 4 : 1 MUX using transmission gates. (4 Marks)

(c) Realize the following logic expressions using CMOS structures:

i) $Y = \overline{A.B.C}$

ii) $Y = A\overline{B} + \overline{A}B$

iii) $Y = \overline{AB + CD}$

iv) $Y = AB + \overline{C}D$

(2+3+3+4=12 Marks)

7. (a) With the help of a flow chart explain the various design steps involved and the fabrication steps involved in successfully siliconising an VLS IC. Identify and briefly explain the various CAD tools used at different stages. (10 Marks)

(b) What is the philosophy of 'Design for testability ? Briefly explain. (4 Marks)

(c) Using sensitized path technique obtain the test vectors and find out the given faults one at a time, for the combinational circuit shown in Fig. Q. 7(c).

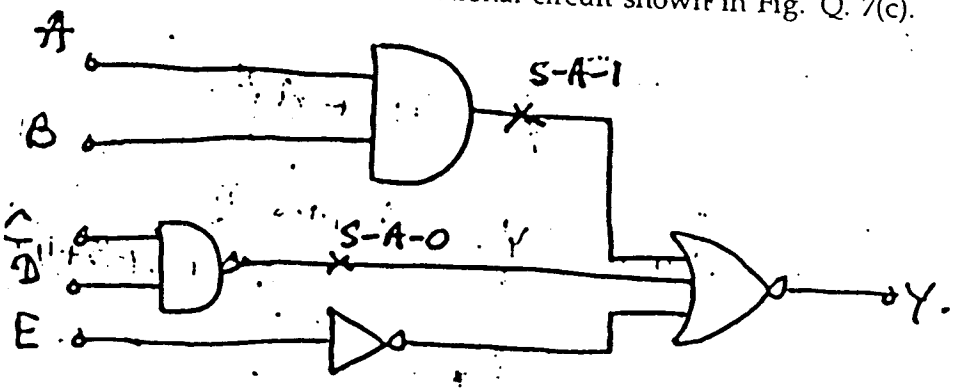

Fig. Q7(c)

(6 Marks)

8. Write short notes on :

i) BiCMOS inverter

ii) Latch - up in CMOS

iii) Scan test

iv) Standard cell based design.

(5 × 4=20 Marks)

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Seventh Semester B.E. Degree Examination, January/February 2004

Electronics and Communication Engineering

VLSI Design

Time: 3 hrs.] [Max. Marks : 100

Note: *1. Answer any FIVE full questions.*
2. Missing data may be suitably assumed.

1. (a) With the help of transfer characteristics bring out the differences in transistor structures and actions of depletion and enhancement type of transistors. (10 Marks)

   (b) With the help of neat diagrams, explain the important stages of N - well CMOS inverter fabrication. (10 Marks)

2. (a) Starting from fundamentals deduce an expression for the drain current Ids of an enhancement type NMOSFET operating in the saturation region. (10 Marks)

   (b) Discuss the various parameters on which the threshold voltage of a MOS transistor depends on. (10 Marks)

3. (a) Show that the Z - ratio of a NMOS inverter driven by an another NMOS inverter through one or more pass transistors is given by 8 : 1. (10 Marks)

   (b) Explain the working of a CMOS inverter with the help of transfer and current versus input voltage characteristics. (10 Marks)

4. (a) Write a 2 I/P NOR CMOS gate and draw the monocrhrome stick diagram for the same. (2+4=6 Marks)

   (b) What do you understand by λ - based design rules ? Illustrate with 3 examples. (2+3= 5 Marks)

   (c) Draw and briefly explain the layout diagram for a burried contact. (4 Marks)

   (d) Define the following.

   i) Sheet resistance

   ii) Standard unit capacitance $\square$ C_g

   iii) The delay unit 'Z' (2+2+1=5 Marks)

5. (a) Deduce pair delay expressions in terms of 'Z' for NMOS and CMOS inverters. (3+4=7 Marks)

   (b) Differentiate the 3 different scaling models applying the scaling rule for the

   i) Static power dissipation

   ii) Gate delay

   iii) No. of components (9 Marks)

Contd.... 2

(c) An off chip capacitance load of 20PF is to be driven from CMOS inverters. For $5\mu m$ technology, deduce the suitable arrangement of inverter and hence compute the overall delay of this inverters arrangement, when the input is

i) ΔV_{in} ii) ∇V_{in} **(8 Marks)**

6. (a) Substantiate with proper relations the limitations of substrate doping and depletion width scaling. **(8 Marks)**

(b) Explain the structured design of Bus arbitration logic for n-line bus with stick diagram. **(8 Marks)**

(c) Draw the switch logic arrangement for transmission gates. **(4 Marks)**

7. (a) Discuss the general considerations of VLSI design process. Illustrate it with an example. **(12 Marks)**

(b) Discuss the significance of regularity in VLSI subsystems. Give the numerical values of regularity for 4 x 4 and 8 x 8 shift register. **(8 Marks)**

8. Write short notes on the following : **(5×4=20 Marks)**

i) Thermal aspects of VLSI processing

ii) CAD tools for design and simulation

iii) Latch up in CMOS circuits

iv) Test and testability

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Seventh Semester B.E. Degree Examination, January/February 2005

Electronics and Communication Engineering

VLSI Design

Time: 3 hrs.] Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) What is Moore's law? Explain this law in the context of evolution of microelectronics. (6 Marks)

   (b) With the help of transfer and output characteristics, explain the working of MOS enhancement mode transistor. (6 Marks)

   (c) Describe with neat sketches the fabrication of N-well CMOS inserter. (8 Marks)

2. (a) Starting from fundamentals, derive an expression for the drain current of a nMOS inverter in both saturation and non saturation regions. (8 Marks)

   (b) Use this equation to obtain $I_{ds}V/sV_{ds}$ characteristics of the device in saturation and non-saturation region. Identify the regions of operation. (4 Marks)

   (c) Explain the working of a CMOS inverter with the help of transfer characteristics. List the variation of the current drawn by the inverter over the entire input swing (8 Marks)

3. (a) Show that $Z_{pu} \mid Z_{pd}$ for an nMOS inverter driven by another nMOS inverter is 4:1. (8 Marks)

   (b) Discuss alternate forms of pull up in basic MOS transistors along with circuit diagram and transfer characteristics. (8 Marks)

   (c) Discuss the characteristic features of BiCMOS inverters. (4 Marks)

4. (a) Draw the circuit diagram and stick diagram of a 3 input NAND gate in both nMOS design style and CMOS design style. (12 Marks)

   (b) Narrate the Lambda based design rules for the following layers:

   i) Polysilicon

   ii) Metal - 1 to polysilicon contact cut

   iii) nMOS depletion transistor

   iv) Diffusion (8 Marks)

5. (a) Justify the statement that CMOS is ratioless inverter. (4 Marks)

   (b) Discuss the significance of sheet resistance R_s and gate capacitance in VLSI technology. (8 Marks)

Contd.... 2

(c) A CMOS NAND 2 is designed using identical NMOSFETs with a value of $\beta_n = 2\beta_p$; the PMOSFETs are of the same size. Given that $V_{DD} = 5V$, $V_{Tn} = 0.6V$ and $V_{Tp} = -0.7V$.

i) Find the mid point voltage V_M for the case of simultaneous switching.

ii) For an NAND2 with $\beta_n = \beta_p$, what would be the midpoint voltage V_M?

(6 Marks)

7. (a) Design a driver chain that will drive a load capacitance of $C_L = 50PF$, if the initial stage has an input capacitance of $C_{in} = 20PF$. Use the correct scaling to determine the number of stages and the relative sizes. Prove the equations that are used for your calculations. Calculate the total delay of the designed driver chain in terms of τ_r. The chain should be a non-inverting one. **(12 Marks)**

(b) Explain an inverting BICMOS driver circuit, with the output voltage levels. **(8 Marks)**

8. (a) What is a Pseudo - NMOS logic circuit ? Give an example. List the merits and demerits of this logic family. **(6 Marks)**

(b) Design a tri-state CMOS circuit that is in a high impedance state when control signal $T = 1$, and acts as a non - inverting buffer when $T = 0$. Explain the circuit. **(4 Marks)**

(c) Compare clocked CMOS with dynamic CMOS logic circuit. **(10 Marks)**

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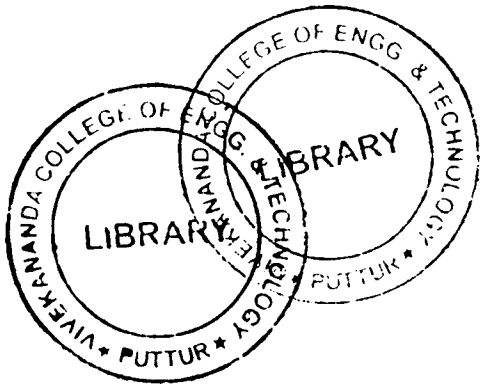


NEW SCHEME

EC74

Reg. No.

Seventh Semester B.E. Degree Examination, January/February 2006

Electronics & Communication Engineering

VLSI Circuits

Time: 3 hrs.) (Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. Missing data may be assumed suitably.

1. (a) Explain the complexity of VLSI chip using the idea of the VLSI Design Funnel. **(6 Marks)**

   (b) Explain the general overview of the VLSI design hierarchy. **(10 Marks)**

   (c) What is Moore's law ? Enumerate it. **(4 Marks)**

2. (a) Consider the two NMOSFETs connected in series as shown in Fig 2.a. Find the V_{out}, for the following values of V_{in}

   i) $V_{in} = 2.9V$

   ii) $V_{in} = 2.5V$

   iii) $4.8V$

   iv) $5.0V$

   Given that $V_{Tn} = 0.5V$

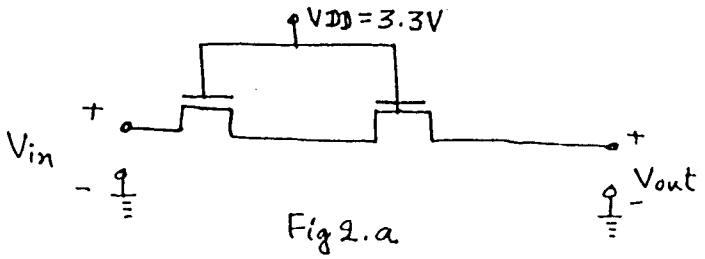


Fig 2.a

   (b) Implement the following gates in CMOS logic. **(5 Marks)**

   i) AOI 22 ii) AOI 321 iii) AOI 212

   iv) OAI 223 v) OAI 211 vi) OAI 12

   (c) Design a 4:1 MUX using transmission gates and explain its operation. **(9 Marks)**

3. (a) With the help of a cross - sectional schematic view of a N - well CMOS process identify the various layers. **(6 Marks)**

   (b) An interconnect line runs over an insulating SiO_2 layer of 10,000 $\mathring{A}$ thick. The line has a width of 0.5 μm and is $40\mu m$ long. The sheet resistance is 25Ω. Find the $\epsilon_{SiO_2} = 3.9$ **(2+5 Marks)**

   i) Line resistance - 'R line'.

   ii) Line capacitance - 'C_{line}'.

Contd.... 2

iii) Line time constant - τ_{line}

(1+2+1=4 Marks)

(c) For an NMOSFET, the following details are available

$\mu_n = 500cm^2/V-sec$; $(V_G - V_{Tn}) = 2.6V.$, $t_{ox} = 100\mathring{A}$

Calculate

i) R_n of the device if $W = 10\mu m$ & $L = 0.5\mu m$

ii) The value of W, if it is required to double the value of R_n calculated in (i).

(2+1=3 Marks)

(d) Design a circuit and layout for a CMOS gate that implements the function

$$Y = \overline{A \cdot B + A \cdot C}$$

(6 Marks)

4. (a) Explain the steps followed to create a new cell that provides the function $F = A \cdot \overline{B}$, starting from the basic X_{NOT}, X_{NAND_2} cells. (6 Marks)

(b) Consider an NMOSFET with an aspect ratio of $(W/L)_n = 4$, that is constructed in a process in which the value of $r = 3.0$. Design the aspect ratio of the PMOSFET that would give the same resistance as that of the NMOSFET. Obtain the relative gate capacitance of the PMOSFET. (4 Marks)

(c) Write the cross-sectional view for the following :

i) Poly contact

ii) Two transistors connected in series,

Draw the respective layouts, including the design rules. (5+5 Marks)

5. (a) Deduce an expression for mid point voltage V_M on the DC characteristic of the CMOS inverter. (8 Marks)

(b) Calculate and sketch the mid point voltage V_M values on the DC characteristic for the following β ratios (Take $V_{DD} = 5V$). Assume $V_{t_n} = \mid V_{tp} \mid = 0.2V_{DD}$;

i) $\beta_n/\beta_p = 1$

ii) $\beta_n/\beta_p = 10$

iii) $\beta_n/\beta_p = 0.1$

(6 Marks)

(c) Derive an expression for the dynamic power dissipated in a CMOS logic circuit. Comment on the ways of reducing this power. (6 Marks)

6. (a) What are pass transistors ? What is the problem with the logic family ? How is it over come through a transmission gate? (6 Marks)

(b) Define the

i) High - to - low time (t_{HL})

ii) Low - to - high time (t_{LH})

Deduce the expression for t_{HL} in terms of τ_n and the expression for t_{LH} in terms of τ_p, where τ_n is the NMOSFET time constant and τ_p is the PMOSFET time constant.

(2+3+3 = 8 Marks)

Contd.... 3

EC74

USN

NEW SCHEME

Seventh Semester B.E. Degree Examination, Dec. 06 / Jan. 07
Electronics and Communication Engineering
VLSI Circuits

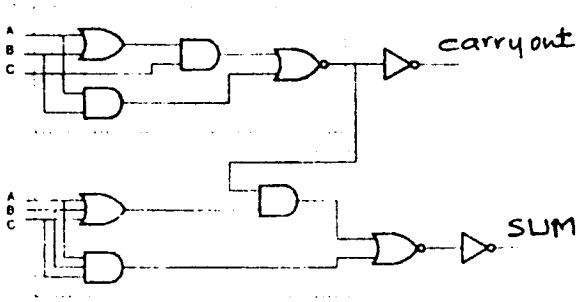
Time: 3 hrs.] [Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Assume typical device parameter values, if necessary.
3. Draw neat diagrams.

1 a. Using flow chart, explain "top-down" and "bottom-up" approach in VLSI design. **(05 Marks)**

b. Realize the following function using CMOS transmission gates:
$F = A.B + \overline{A}\overline{C} + A\overline{B}C$ **(07 Marks)**

c. Figure1(c) is the gate level schematic of one bit full adder circuit. For the given schematic circuit directly map CMOS transistor level circuit. **(08 Marks)**



Gate level schematic of one bit fulladder.

Figure1.c.

2 a. Explain the structural design of CMOS logic circuits. **(04 Marks)**

b. The figure2(b) shows stick diagram layout of the complex CMOS logic gate with an arbitrary ordering of the polysilicon gate columns.
i) Write down the output Boolean function V_{out} of the complex logic gate.
ii) Sketch the CMOS logic gate circuit.
iii) Is it possible to find Euler graph for the circuit? If so construct the graph and use it to obtain optimized stick level layout. **(10 Marks)**

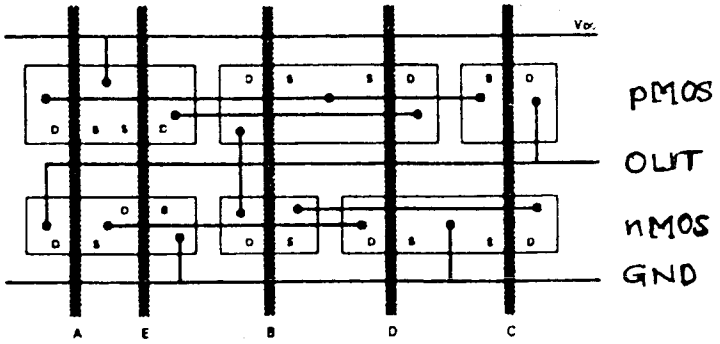


Figure 2.b Stick diagram layout of complex CMOS logic gate.

Contd.... 2

4 a. Explain the steps followed to create a new cell that provides the function $f = a.\bar{b}$ starting from the basic X_{NOT} and X_{NOR2} cells with neat diagrams. **(06 Marks)**

b. Consider a NMOSFET with an aspect ratio of $(W/L)_n = 4$ that is constructed in a process in which the value of r = 3.0. Design the aspect ratio of the PMOSFET that would give the same resistance as that of the NMOSFET. Obtain relative gate capacitance of the PMOSFET. Explain. **(04 Marks)**

c. Implement a simple NOT gate with horizontal FETs. Explain the features with a neat layout. **(10 Marks)**

5 a. Explain the speed versus area trade off in detail in chip design. **(08 Marks)**

b. Calculate and sketch the mid point voltage V_m values on the DC characteristics for the following β ratios. Assume V_{DD}= 5 V and $V_{tn} = |V_{tp}| = 0.7$ V.

i) $\beta_n = \beta_p = 1$

ii) $\beta_n = \beta_p = 10$

iii) $\beta_n = \beta_p = 0.1$ **(06 Marks)**

c. Derive an expression for the power dissipation in a CMOS logic circuit in dynamic state. Comment on the ways of reducing this power. Explain the relation between power dissipation and frequency of operation. **(06 Marks)**

6 a. Explain how NAND2 gate is designed for better transient response with relevant equations and drawings. **(06 Marks)**

b. Define the terms below for an inverter with neat sketches

i) High to Low time (t_{HL})

ii) Low to High time (t_{LH})

Deduce the expression for the t_{HL} in terms of τ_n and the expression t_{LH} in terms of τ_p where τ_n is the NMOSFET time constant and τ_p is the PMOSFET time constant. Explain their complementary nature of NAND2 and NOR2 gates. **(08 Marks)**

c. A CMOS NAND2 is designed using identical NMOSFETs with a value of $\beta_n = 2\beta_p$. The PMOSFETs are of the same size. Given that V_{DD} = 5 V, V_{Tn} = 0.6 V and $V_{tp} = -0.7$ V

i) Find the mid point voltage V_m for the case of simultaneous switching.

ii) What would be the mid point voltage with $\beta_n = \beta_p$? **(06 Marks)**

7 a. Use the logical effort to find a relative size of each stage needed to minimize the delay through the chain shown below. Assume symmetric gates with r = 2.5.

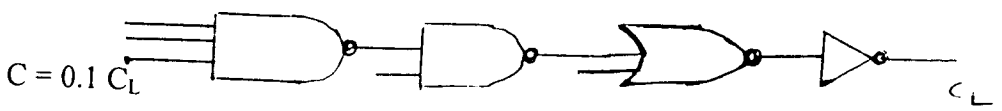


Fig.7(a)

b. Design a digital BiCMOS circuit that implements the function $f = \overline{a + b.c}$ and explain its advantages and disadvantages. **(12 Marks)**

8 a. Draw the pseudo-NMOS inverter circuit and explain its operation with the expression for V_{OL}. **(08 Marks)**

b. Compare clocked CMOS circuits with dynamic logic circuits with neat diagrams with examples. **(06 Marks)**

c. Explain the operation of dual rail logic circuit and draw the circuit for AND/NAND implementation in dual rail logic. **(08 Marks)**

***** **(06 Marks)**

EC74

c. Consider a process that has an oxide thickness of t_{ox} = 9.5 nm. The particle mobilities are given as μ_n = 540 and μ_p = 220 cm^2/V-sec. An nFET and pFET are made, both with W = 12 μm, L = 0.35 μm. Both have gate voltage of V_G = 3.3 V, while the threshold voltages are V_{Tn} = 0.65 V and V_{Tp} = -0.74 V.

i) Find the values of R_n and R_p for the two transistors.

ii) Suppose that we want to keep the nFET the same size, but increases the width of the pFET to the point where $R_p = 0.8R_n$. Find the required width of the pFET.

(06 Marks)

3 a. The simplified layout of a CMOS complex logic circuit is given in figure3(a). Draw the corresponding circuit diagram with its output function. Find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that (W/L)p = 15 for all pMOS transistor (W/L)n = 10 for all nMOS transistors.

(10 Marks)

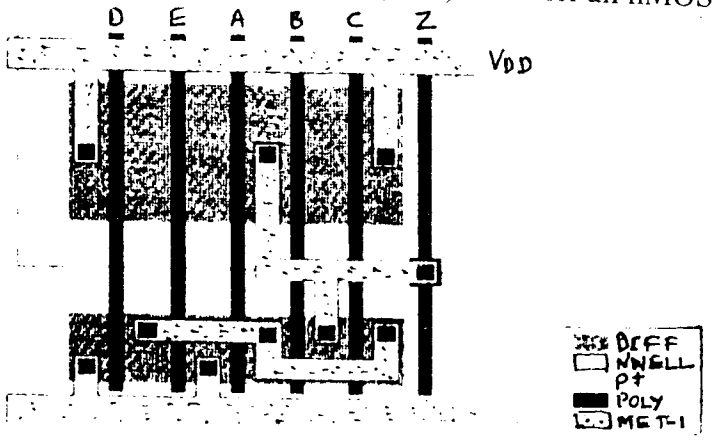


Figure 3.a Layout of a CMOS complex logic circuit

b. Enhancement mode NMOS and PMOS device both have parameters L = 4 μm and t_{ox} = 500 ^{0}A. For the NMOS transistor, V_{TN} = +0.6 V, μ_n = 675 cm^2/V-s, and the channel width is W_p: for the PMOS transistor, V_{TP} = -0.6 V, μ_p = 375 cm^2/V-s, and the channel width is W_p. Design the width of two transistors such that they are electrically equivalent and the drain current in the PMOS transistor is I_D = 0.8 mA when it is biased in the saturation region at V_{SG} = 5 V. What are the values of β_n, β_p, W_n and W_p?

(10 Marks)

4 a. Derive an expression for midpoint voltage V_m, and (β_n/β_p), of a CMOS inverter circuit. What is the design equation of (β_n/β_p) for a symmetrical inverter VTC? Discuss the dependence of V_m on the device ratio. **(10 Marks)**

b. Explain the power dissipation in a CMOS inverter circuit. **(05 Marks)**

c. A CMOS digital logic circuit contains the equivalent of 2 million CMOS inverters and biased at V_{DD} = 5 V. The equivalent load capacitance of each inverter is 0.4 pF and each inverter is switching at 150 MHz. Determine the total average power dissipated in the circuit. **(05 Marks)**

Contd.... 3

EC74

5 a. For a CMOS NAND2 logic gate, obtain the value of the midpoint voltage V_m for the case of simultaneous using layout drawings. Discuss the effect on VTC due to simultaneous switching. **(10 Marks)**

b. Consider the CMOS transmission gate as shown in figure5(b). Assume transistor parameters of V_{Tn} = +0.8 V and V_{Tp} = -1.2 V. When Φ = 5 V, input V_I varies with time as V_I = 0.5t V for $0 \leq t \leq 10$ s. Let $V_0(t = 0) = 0$ and assume C_L = 1 pf. Determine the range of times that the NMOS and PMOS devices are conducting or cut off. **(10 Marks)**

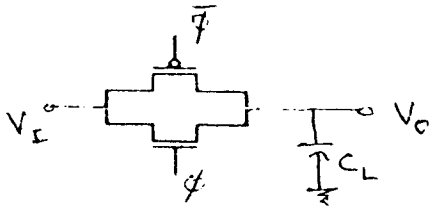


Figure 5.b CMOS Transmission gate.

6 a. Discuss the concept of delay minimization in inverters in cascade. Obtain the expression to determine number of states "N", scaling factor "S" and total minimum time needed for the signal to reach the load C_L. **(12 Marks)**

b. Explain the operation of BiCMOS driver circuit used to drive high capacitance output load C_L. Compare the time delay of BiCMOS with CMOS with respect to output load capacitance C_L. **(08 Marks)**

7 a. Draw the circuit diagram for a dynamic logic gate that has an output of $f = \overline{(a.b + c.a)}$ using smallest number of transistors. Explain and evaluate precharging mode of operation. **(08 Marks)**

b. What is charge sharing phenomenon in dynamic logic circuit? **(04 Marks)**

c. Why Domino CMOS logic circuit is called high performance dynamic CMOS circuit? Explain how this circuit eliminates the cascading problem of dynamic CMOS circuit. What are the advantages and limitations of this circuit? **(08 Marks)**

8 Write short notes on:

a. Clocking and data flow control

b. Layout and stick diagram

c. MOSFET capacitances

d. Pseudo nMOS logic. **(20 Marks)**

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NEW SCHEME

Seventh Semester B.E. Degree Examination, May 2007
Electronics and Communication Engineering
VLSI Circuits

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain "The magic technology funnel" in relation to VLSI manufacturing industry. **(06 Marks)**

b. Explain the design flow for microprocessor chip in detail. **(10 Marks)**

c. Explain Moore's law in the evolution of VLSI chips over the years graphically. **(04 Marks)**

2 a. Consider the two MOSFETs connected in series as shown in Fig.2(a). Find V_{OUT} for the following values of V_a and V_b. Assume $V_{Tn} = 0.6$ V.

i) $V_a = 3.3$ V and $V_b = 3.3$ V
ii) $V_a = 0.5$ V and $V_b = 3.0$ V
iii) $V_a = 2.0$ V and $V_b = 2.5$ V
iv) $V_a = 3.3$ V and $V_b = 1.8$ V

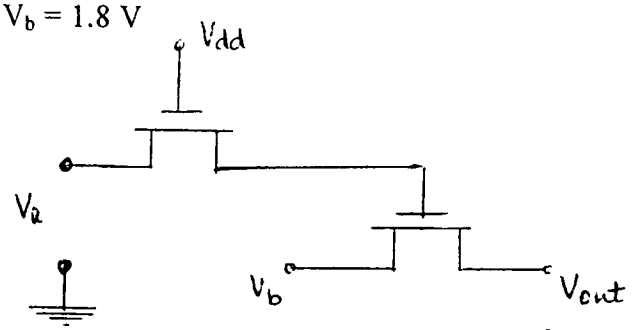

Fig.2(a)

Explain your answers. **(06 Marks)**

b. Explain the concept of bubble pushing to build the PFET array of a MOSFET circuit. Using the technique build a CMOS circuit for the logic expression $f = \overline{(a.b) + (c.d) + e}$ **(08 Marks)**

c. Design a 2 : 1 MUX using transmission gates and explain its operation. **(06 Marks)**

3 a. With the help of a cross sectional schematic view of N well C-MOS process, identify the various layers. **(07 Marks)**

b. An interconnect line runs over an insulating SiO_2 layer of 10,000 Å thick. The line has a width of 0.5 μm and is 40 μm long. The sheet resistance is 25 Ω. Find the following if $\varepsilon_{SiO_2} = 3.9$.

i) Line resistance – R_{line}
ii) Line capacitance – C_{line}
iii) Line time constant – τ_{line} **(04 Marks)**

c. For PMOS FET, the following details are available. $\mu_p = 500$ cm^2/v-sec, $(V_G - |V_{TP}|) = 2.6$ V. $t_{OX} = 100$ Å calculate with $\varepsilon_{SiO_2} = 3.9$

i) R_p of the derive if w = 10 μm and L = 0.5 μm
ii) The value of w, if it is required to double the value of R_p. **(03 Marks)**

d. Design a circuit and draw the layout for a CMOS gate that implements the function $f = \overline{a.b.(c + d)}$ **(06 Marks)**

Contd.... 2

An inverter users FETs with $\beta_n = 2.1$ mA/V^2 and $\beta_p = 1.8$ mA/V^2. The threshold voltages are given as $V_{Tn} = 0.60$ V and $V_{Tp} = -0.70$ V and the power supply has a value of $V_{DD} = 5$ V. The parasitic FET capacitance at the output node is estimated to $C_{FET} = 74$ fF.

i) Find the mid point voltage V_m ii) Find the values of R_n and R_p

iii) Calculate the rise and fall times when an external load of value of C_L 115 fF is connected to the output. **(09 Marks)**

Compare and comment on VTC of NAND and NOR gates. **(04 Marks)**

With respect to CMOS NAND circuit, explain how switching delays increase with fan-in and external load. **(08 Marks)**

An OAI function of the form $f = \overline{(a+b).(b+c).d}$ is built using series parallel CMOS structuring:

i) Design the circuit

ii) An inverter with $\beta_n = \beta_p$ is used as a sizing reference. Find the transistor sizes needed to equalize the path resistances in both the nFET and pFET chain.

iii) Expand the function into AOI form, and apply the same sizing philosophy. Which design (the AOI or the OAI) requires the smallest total transistor area? **(12 Marks)**

Analyze the delay through the chain of inverters to drive large capacitance load. Derive necessary equations to obtain total delay, (N) number stages in cascade, (S) scaling factor for a minimum delay chain. Clearly mention the assumption made during the analysis. **(08 Marks)**

Consider the logic chain shown in Fig.Q6(b). The input at A is switched from a '0' to a '1'. Find an expression for the delay time through the chain. **(09 Marks)**

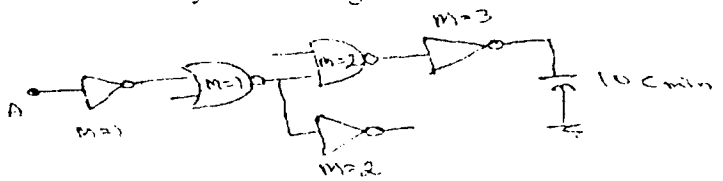

Fig.Q6(b)

Define the following:

i) Logical effort ii) Electrical effort iii) Path effort. **(03 Marks)**

Design a driver chain that will drive a load capacitance of $C_L = 40$ pF if the initial stage has an input capacitance of $C_{in} = 50$ fF. Use ideal scaling to determine the number of stages and the relative sizes. **(08 Marks)**

Explain the function of BiCMOS driver circuit. Mention the advantages and disadvantages of BiCMOS circuits. Compare the performance BiCMOS and CMOS circuits in driving external load capacitance. **(08 Marks)**

Construct a BiCMOS NOR2 circuit. **(04 Marks)**

Draw the pseudo nMOS circuit to provide the function $f = \overline{(a.b+c)}$. List the merits and demerits of this logic family. **(08 Marks)**

Consider a CMOS process that is characterized by $V_{DD} = 5$ V, $V_{Tn} = 0.7$ V, $V_{Tp} = -0.85$ V, $K'_n = 120$ μA/V^2 and $K'_p = 55$ μA/V^2. A pseudo nMOS inverter is designed using a nFET aspect ratio of 4. Find the pFET aspect ratio needed to achieve $V_{OL} = 0.3$ V. **(06 Marks)**

Drew the circuit diagram for a dynamic logic gate that has an output of $F = \overline{a(b+c+d)}$. What is the effect of charge sharing on the output of the circuit? **(06 Marks)**

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EC74

Seventh Semester B.E. Degree Examination, Dec.07 / Jan.08
VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Explain the significance of the following with respect to VLSI Design:
i) Moore's Law ii) Full custom and Semi Custom IC Design iii) VLSI design hierarchy. (09 Marks)

b. Determine the V_{out} of the following circuits shown in FigQ1(b)I and Fig.Q1(b)ii when $V_{DD} = 3.3$ V, $V_{Tn} = 0.6$ V, $V_{Tp} = |0.6V|$, $V_a = 3.3$ V and $V_b = 1.8$ V. (06 Marks)

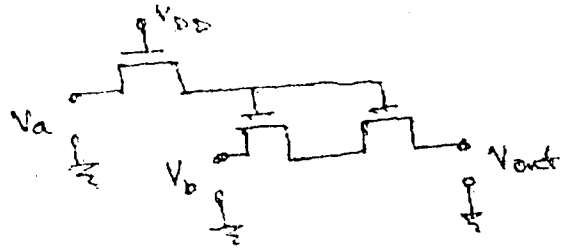

Fig.Q1(b)i

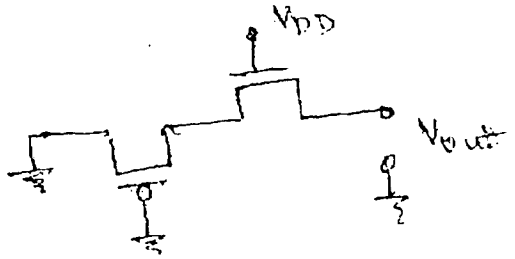

Fig.Q1(b)ii

c. Design a CMOS logic gate for the function $F = G[A[[B(C+D)]+E]+F]$. (05 Marks)

2 a. What do you understand by structural CMOS logic design? Explain how structured logic design concept helps in designing CMOS complex logic circuits. (08 Marks)

b. Realize clocked SR latch (NOR2) in AOI CMOS structure. (05 Marks)

c. For the logic diagram of Fig.Q2(c), draw a neat CMOS layout using Euler method. (07 Marks)

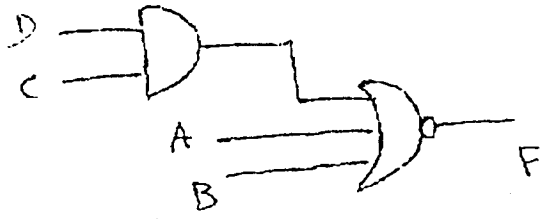

Fig.Q2(c)

3 a. In terms of terminal voltages of 'p' and 'n' FETs, write the relationships between voltages for the three regions of operation of a CMOS inverter. (Assume V_{tn} and V_{tp} are threshold voltages of n and p FETs respectively). Neglect V_{sb}. (06 Marks)

b. Consider a process that has an oxide thickness $t_{ox} = 9.5$ nm. The particle mobilities are given as $\mu_n = 540$ and $\mu_p = 220$ cm^2/V sec. An nFET and a pFET are made, both with $W = 12$ μm, $L = 0.35$ μm. Both have gate voltages of $V_G = 3.3$ V, while the threshold voltages are $V_{tn} = 0.65$ V and $V_{TP} = -0.74$ V.
i) Find the values of Rn and Rp for the two transistors.
ii) Suppose that we want to keep the nFET the same size, but increase the width of the pFET to the point where $R_p = 0.8$ Rn. Find the required width of the pFET. (07 Marks)

c. With the help of a cross sectional schematic view of a N-well CMOS process identify the various layers. Discuss the metal interconnect layers with a neat schematic. (07 Marks)

4 a. Briefly explain the power dissipation in CMOS gates. Compare the chip power for two cases. In one case, a chip has 10 M gates, an activity factor of 10%, $V_{DD} = 1.8$ V, a clock frequency of 500 MHz and an average capacitance per node of 20 fF. In the second case, a chip has 50 M gates, an activity factor of 5%, $V_{DD} = 1.2$ V, a clock frequency of 1 GHz and average capacitance per mode of 10 fF. Which design is better? (07 Marks)

6 a. Derive an expression for rise time and fall time of an inverter along with propagation delay. **(08 Marks)**

b. An inverter uses FETS with $\beta_n = 2.1mA/V^2$, $\beta_P = 1.8mA/V^2$, $V_{Tn} = 0.60V$, $V_{TP} = -0.70V$ and the power supply has $V_{DD} = 5.0V$. The parasitic FET capacitance at the output node is estimated to be $C_{FET} = 74fF$. Find the midpoint voltage V_M value of R_n and R_P.

i) Calculate rise and fall times at the output when $C_L = 0$.

ii) Calculate rise and fall times when an external load of $C_L = 115fF$ is connected to output.

iii) Plot t_r and t_f as a function of C_L. **(08 Marks)**

c. Comment on size of 3 input gate: i) NAND3 gate. ii) NOR3 gate. **(04 Marks)**

7 a. Derive an expression for the minimization of delay in an inverter cascade. **(12 Marks)**

b. Analyze the logic cascade using the technique of logical effort for figure Q7 (b). Assume $C_4 = 500fF$ and $C_1 = 20fF$, $r = 2.5$. Find the path logical effort, path electrical effort, path effort and total path delay. **(08 Marks)**

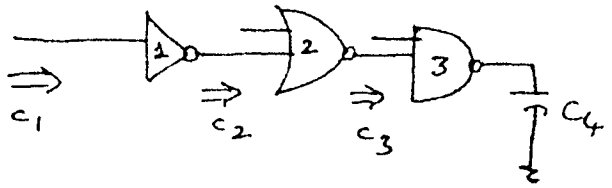

Fig. Q7 (b)

8 a. Explain Pseudo NMOS circuit with an example and explain the features of pseudo NMOS circuit. **(08 Marks)**

b. Explain clocked CMOS (C^2MOS) logic gate and explain in detail the charge leakage problem. **(08 Marks)**

c. Draw the circuit diagram for a dynamic logic gate that has an output of $f = \overline{(a.b + c.a)}$. **(04 Marks)**

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EC74

Seventh Semester B.E. Degree Examination, May/June 08
VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain how digital VLSI chips are classified by the approach used to implement and build the circuit. Give a suitable example for each. **(09 Marks)**

b. With a diagram explain how a bonding pad is used to interface system on chip [SOC] to other components to create an operational unit. **(06 Marks)**

c. Explain nFET pass characteristics in brief. **(05 Marks)**

2 a. Implement the following functions using transmission gates:

i) $F = a \oplus b$

ii) $F = \overline{a \oplus b}$ **(06 Marks)**

b. Design a cMOS circuit for the AOI expression, $F = \overline{a + b \cdot (c + d)}$. **(08 Marks)**

c. Apply bubble-pushing to the following AOI logic diagram (with nFETs) to convert in to the topology of the pFET array. **(06 Marks)**

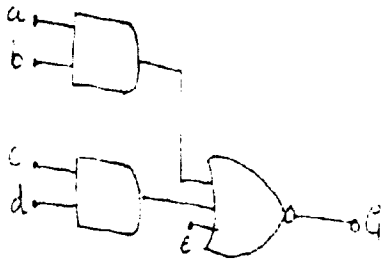

Fig. Q2 (c) AOI Logic diagram

3 a. For an n-channel MOSFET explain the followings

i) Parallel-plate capacitance concept.

ii) Gate capacitance concept. **(08 Marks)**

b. Consider the AOI expression.

$F = \overline{x \cdot y + z \cdot w}$

Design the cMOS logic gate and then construct a basic layout for the circuit. **(08 Marks)**

c. Calculate the gate capacitance of the FET if $tox = 50A^{\circ}$, $\epsilon_0 = 8.854 \times 10^{-14}$ F/cm, $A_G = 4 \times 10^{-9} cm^2$. **(04 Marks)**

4 a. Explain different reasons for latch-up condition in a cMOS technology. Discuss different prevention techniques available to avoid latch up in

i) Bulk cMOS technology.

ii) Non-bulk cMOS technology. **(09 Marks)**

b. Discuss the importance of the following CAD toolsets in the physical design,

i) Layout versus schematic [LVS].

ii) Design rule checker [DRC].

iii) Electrical rule checker [ERC]. **(06 Marks)**

c. An nFET with the following parameters is available : Aspect ratio = 4, C_{Gn}= 13.8 fF, μ_n = 520 cm^2/v-sec, μ_p = 490 cm^2/v-sec. Create a pFET with the same resistance and also calculate the gate capacitance of the pFET. **(05 Marks)**

5 a. For a cMOS integrated circuit, derive an equation for the total power dissipation in terms of dc power and dynamic power. **(10 Marks)**

b. For a cMOS inverter, explain the following, i) DC analysis ii) Transient analysis. **(06 Marks)**

c. A pFET with the following parameters is available $K'_p = 62\ \mu A/V^2$, V_{TP} = -0.85 V, Aspect ratio = 8, Output capacitance = 150 fF. Calculate the pFET resistance and time constant. **(04 Marks)**

6 a. For an nFET pass transistor, derive a relation for a rise time and fall time for logic 1 transfer and logic 0 transfer respectively. **(10 Marks)**

b. Draw the circuit of a transmission gate RC model and explain how resistances and capacitances are obtained. **(05 Marks)**

c. Calculate the activity coefficient in the following two gates:

i) NOR 2 gate with $P_0 = ¾$ and $P_1 = ¼$

ii) NAND 2 gate with $P_0 = ¼$ and $P_1 = ¾$ **(05 Marks)**

7 a. Draw a structure of a clocked cMOS gate and explain its operation. **(10 Marks)**

b. Explain why charge keeper circuits are required in the domino cascade. With a diagram explain any one charge – keeper circuit. **(06 Marks)**

c. Calculate the hold time t_h in a clocked cMOS gate corresponding to the maximum time that the logic 1 voltage can be stored if the output capacitance is 50 fF, leakage current is 0.1 pA and the voltage change is 1V. **(04 Marks)**

8 a. Draw the circuit of an inverting Bicmos driver and explain it's operation as i) NOT logic ii) Switching iii) DC operation. **(10 Marks)**

b. Define and explain the logical effort of a logic gate. **(04 Marks)**

c. Design a driver chain that will drive a load capacitance of CL = 40 pF if the initial voltage has an input capacitance of Cin = 50 fF. Use ideal scaling to determine the number of stages and the relative sizes. **(06 Marks)**

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